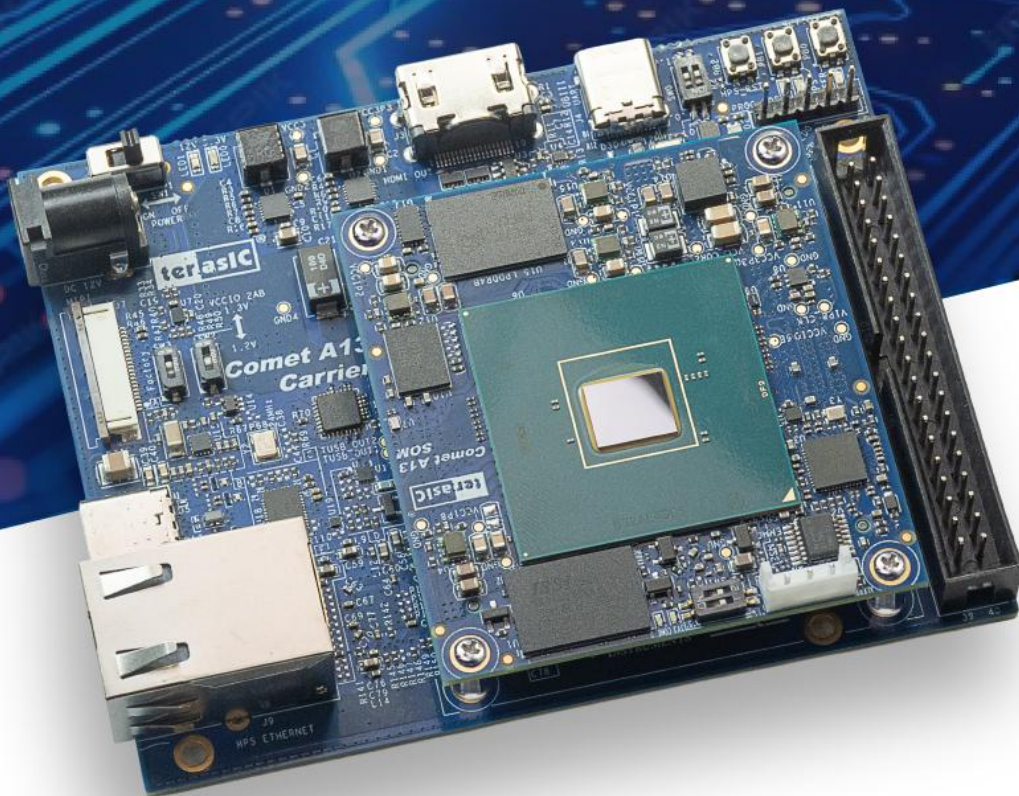


Comet A13



Carrier Board Design Guide

CONTENTS

CHAPTER 1 ABOUT THIS GUIDE	3
CHAPTER 2 POWER AND RESET.....	4
2.1 GENERAL POWER REQUIREMENTS	4
2.2 POWER-UP SEQUENCE	4
2.3 POWER ENABLE SIGNALS.....	5
2.4 POWER STATUS SIGNALS	6
CHAPTER 3 COMET A13 BOARD INTERFACE	7
3.1 MODULE CONNECTORS	7
3.2 TRANSCEIVERS	7
3.3 JTAG INTERFACE	8
3.4 LVDS PIN PLACEMENT RESTRICTIONS	8
3.5 HPS I/O PIN ASSIGNMENTS	10
3.6 RESET SIGNALS	11
3.7 BOOT CONFIGURATION SIGNALS	11
3.8 TRACE-LENGTH MATCHING BETWEEN SOM AND CARRIER BOARDS	12
CHAPTER 4 MECHANICAL AND HEATSINK DESIGN.....	13
4.1 INTRODUCTION	13
4.2 HEAT SPREADER	13
4.3 MECHANICAL DIMENSIONS.....	13
4.4 BOARD-TO-BOARD (B2B) CONNECTOR ORIENTATION AND PLACEMENT	19
CHAPTER 5 ASSEMBLY & DISASSEMBLY.....	21
5.1 ASSEMBLY & DISASSEMBLY FOR SOM AND CARRIER.....	21
5.2 3D CAD FILES.....	21
CHAPTER 6 POWER CONSUMPTION MEASUREMENT.....	22
6.1 POWER MONITORING SYSTEM	22
ADDITIONAL INFORMATION.....	23

Chapter 1

About this Guide

This document provides guidelines for designing a custom carrier board compatible with the Comet A13 Agilex 5 SoC SOM. It includes information on power-up sequencing, control signal management, JTAG connection, EEPROM programming, HPS I/O constraints, and connector pin assignments.

Chapter 2

Power and Reset

2.1 General Power Requirements

The carrier board must provide the following power rails :

Table 1-1 Part Number of the connector on the Titan S10 SOM

Pin Name	Description	Voltage
VIN	Power input to the SOM.	5V ~ 12V
VCCIO_xx	FPGA VCCIO rails supplied at voltage levels appropriate for the FPGA I/O standards in use. These FPGA VCCIO rails should be enabled by GROUP3_PWR_EN signal, the soft-start time of these FPGA VCCIO rails should between 1 msec and 3 msec.	User Defined
VCC5_FAN	Power input for the SOM cooling fan.	5V

2.2 Power-Up Sequence

The power-up sequence is critical. The carrier board must respect the ramp times (1 to 3 msec for FPGA VCCIO rails)

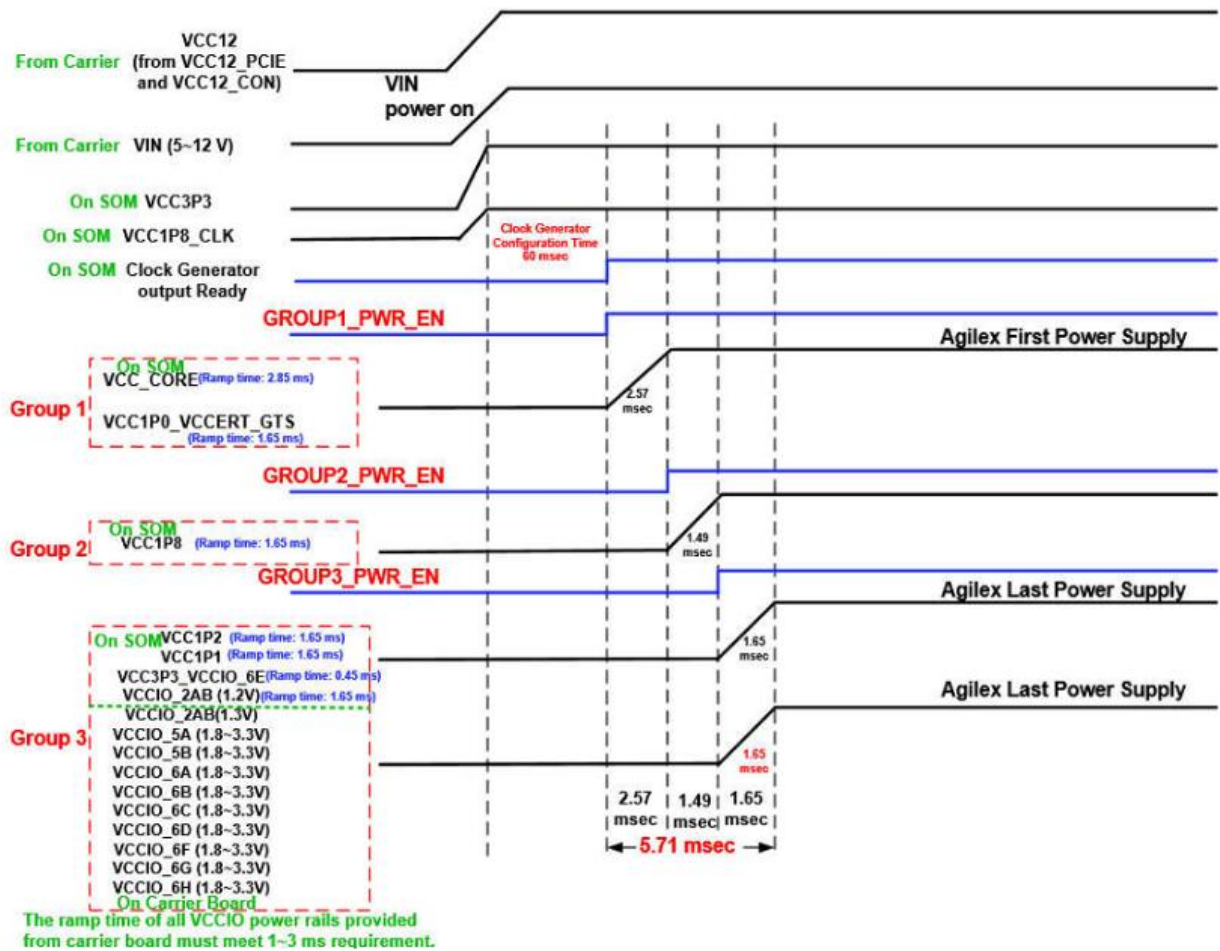


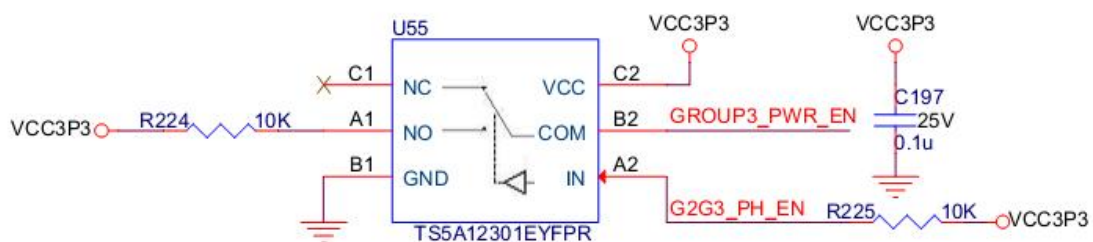
Figure 2-1 Power Up Sequence for Comet A13 SOM and Carrier Board

2.3 Power Enable Signals

- **GROUP2_PWR_EN**: Enables the 1.8V power supply for HPS peripheral devices on the carrier board.
- **GROUP3_PWR_EN**: Enables the FPGA VCCIO power rails on the carrier board.
- **VCCIO_2AB_1V2_EN**: Configures the VCCIO voltage of FPGA sub-bank 2AB to 1.2 V or other I/O standards required by the user application (1.0 V, 1.05 V, 1.1 V, or 1.3 V)
 - ◆ Logic High: VCCIO_2AB of the FPGA is set to 1.2V, supplied by the SOM.
 - ◆ Logic Low: VCCIO_2AB of the FPGA is set to other I/O standards required by the user application, supplied by the carrier.

2.4 Power Status Signals

- **VCCIO_CARRIER_PG:** Power-good signal asserted when all FPGA VCCIO rails on the carrier board are operating normally. This signal informs the SOM that all carrier-provided VCCIO power rails are ready.
- **G2G3_PH_EN:** Detection signal used to identify SOM insertion.
 - ◆ Should be connected to J2 pin-D49. The J2 pin-D49 on SOM is connected to GND. This G2G3_PH_EN signal must be pulled high on the carrier board.
 - ◆ When the G2G3_PH_EN signal is pulled high, GROUP2_PWR_EN and GROUP3_PWR_EN are also pulled high, allowing the carrier power rails to be enabled even without the SOM installed.
 - ◆ This enables verification of all carrier power rails before SOM insertion.
 - ◆ The following is the design example for G2G3_PH_EN :



IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L or Open	ON	OFF
H	OFF	ON

When G2G3_PH_EN is pulled high, GROUP2_PWR_EN and GROUP3_PWR_EN are also pulled high, enabling verification of carrier rails even without the SOM installed

Comet A13 Board Interface

3.1 Module Connectors

The Comet A13 SOM connects to the carrier board via high-density **B2B** connectors.

- **Carrier Board Connector:** Samtec SEAF8, 400-pin female connector (P/N: SEAF8-50-05.0-S-08-3)
- **SOM Connector:** Samtec SEAM8, 400-pin male connector (P/N: SEAM8-50-S02.0-S-08-3)

With the recommended connectors, the stack height between the Comet A13 SOM and the carrier board is **7 mm**.

For detailed pinout assignments of the B2B connectors (J1 and J2), please refer to the pinout tables provided in the engineering documentation: [Comet_A13_Pinout.xlsx](#).

3.2 Transceivers

Connectors J1 and J2 each provide two pairs of transceiver reference clock pins, allowing the carrier board to supply the necessary clock signals to the FPGA transceivers.

Design and Layout Guidelines:

- **Placement Rules:** For detailed information on transceiver channel placement rules and design requirements, please refer to Chapter 2.2 of the [GTS Transceiver PHY User Guide](#).
- **Unused Pin Termination:**
 - a) **Reference Clocks:** If the provided reference clock pins on J1 and J2 are not used in the application, they must be tied to ground (GND). For example, if users need to provide a transceiver reference clock from the carrier board to the SOM, they can route the desired clock to **J1_GTSL1A_REFCLK**.

However, if the on-board 100 MHz **GTSL1A_REFCLK_100M** reference clock on the SOM meets the user's transceiver application requirements and the carrier board does not need to provide an additional reference clock to **J1_GTSL1A_REFCLK**, then

J1_GTSL1A_REFCLK must be tied to ground.

- b) **Input Pins:** Any unused transceiver input pins must also be terminated by connecting them to **ground**.

3.3 JTAG Interface

To enable FPGA configuration, the four JTAG signals must be connected to either a standard 2x5 JTAG pin header or an on-board USB Blaster interface.

- **IO Standard:** Please note that the FPGA JTAG interface operates at 1.8V.
- **Reference Design:** A design example for the 10-pin JTAG header implementation is shown below.

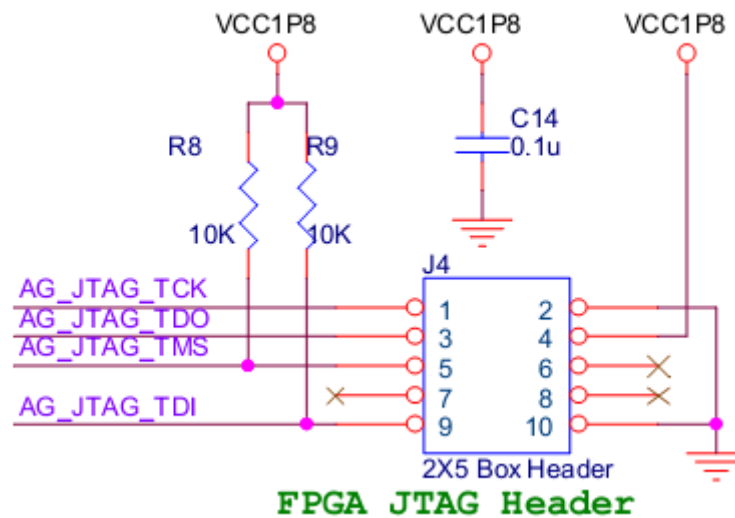


Figure 3-1 USB Blaster III shown in PC Device Manager

3.4 LVDS Pin Placement Restrictions

This section informs users that certain HSIO 2A and 3A I/Os of the FPGA on the J1 and J2 connectors cannot be configured as LVDS signals. Please take note of these restrictions when designing the carrier board. The restricted nets are listed in the table below.

Table 3-1 Restricted HSIO 2A, and 3A Nets on J1/J2 Connectors (LVDS Unavailable)

FPGA Bank	Restricted Carrier Board Net Names
2A	J1_HSIO_2AB_A_p4 / n4
	J1_HSIO_2AB_A_p1 / n1
3A	J2_HSIO_3AT_A_p16 / n16
	J2_HSIO_3AT_A_p13 / n13

The detailed reasons for these restrictions are described below:

According to Altera Agilix 5 LVDS SERDES User Guide, there are Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in the Same HSIO Bank. As shown in the figure below, since 2A bank index 50/54 is assigned to LPDDR4 for single-ended use, the two pairs at 2A index 40/41 and 46/47 cannot be used for LVDS. Correspondingly in the carrier board schematic, the pairs J1_HSIO_2AB_A_p4 / J1_HSIO_2AB_A_n4 and J1_HSIO_2AB_A_p1 / J1_HSIO_2AB_A_n1 cannot be assigned as LVDS signals.

When the LPDDR4A port is used as the HPS DDR4 interface, all I/O pins in I/O Lanes 5 and 6 of the 3A bank become unavailable under both HPS EMIF mapping scenarios: “Using only the F2H bridge” and “Both bridges are used.”

Aside from these two HPS EMIF-mapping scenarios, all I/O pins in I/O Lanes 5 and 6 of the 3A bank become available. Since the VCCIO of bank 3A is fixed at 1.1 V, the 12 differential pairs in I/O Lanes 5 and 6 can only be used as LVDS RX or single-ended signals. When using them as LVDS RX, as shown in the figure below, because 3A bank index 74/78 is assigned to LPDDR4 for single-ended use, the pairs at 3A index 64/65 and 70/71 cannot be used as LVDS RX. Correspondingly in the carrier board schematic, the pairs J2_HSIO_3AT_A_p16 / J2_HSIO_3AT_A_n16 and J2_HSIO_3AT_A_p13 / J2_HSIO_3AT_A_n13 cannot be assigned to LVDS RX signals.

Table 19. Restricted Pin Placement Combinations for True Differential and Single-Ended I/O Standards in the Same HSIO Bank

This table lists the combinations of pins and I/O standards not allowed in the same HSIO bank. Examples:

- If you place a true differential I/O standard in pin pair 10 and 11, do not place single-ended I/O standards in pins 8 or 19.
- If you place a single-ended I/O standard in pin 57 or 67, do not place a true differential I/O standard in pin pair 58 and 59.

Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)		Combinations Not Allowed (Pin Index Number)	
True Differential Pin Pair	Single- Ended Pin	True Differential Pin Pair	Single- Ended Pin	True Differential Pin Pair	Single- Ended Pin	True Differential Pin Pair	Single- Ended Pin
0 and 1	3, 4	24 and 25	27, 28	48 and 49	51, 52	72 and 73	75, 76
2 and 3	0	26 and 27	16, 24	50 and 51	40, 48	74 and 75	64, 72
4 and 5	1, 15	28 and 29	25, 39	52 and 53	49, 63	76 and 77	73, 87
6 and 7	9	30 and 31	22, 32	54 and 55	46, 56	78 and 79	70, 80
8 and 9	6, 11	32 and 33	31, 34	56 and 57	55, 58	80 and 81	79, 82
10 and 11	8, 19	34 and 35	33, 43	58 and 59	57, 67	82 and 83	81, 90
12 and 13	14, 17	36 and 37	38, 41	60 and 61	62, 65	84 and 85	86, 89
14 and 15	5, 12	38 and 39	29, 36	62 and 63	53, 60	86 and 87	77, 84
16 and 17	13, 26	40 and 41	37, 50	64 and 65	61, 74	88 and 89	85
18 and 19	10, 21	42 and 43	35, 45	66 and 67	59, 69	90 and 91	83, 92
20 and 21	18, 23	44 and 45	42, 47	68 and 69	66, 71	92 and 93	91, 94
22 and 23	20, 30	46 and 47	44, 54	70 and 71	68, 78	94 and 95	93

Figure 3-2 Restricted Pin Placement Combinations for True Differential and Single-Ended I/O

3.5 HPS I/O Pin Assignments

To ensure that the carrier board's HPS pin assignments comply with Altera Agilex 5 specifications, users must adhere to the rules defined in the official pin information documentation. Specifically, HPS peripheral interface pin assignments must be arranged according to the "**Hard Processor System Pin Information for Agilex 5 Devices**" Excel spreadsheet.

Reference Document: Please download the pin information spreadsheet from the following link:
[Hard Processor System Pin Information for Agilex 5 Devices](#) .

Important Notes:

- **Fixed SD/eMMC Pins:** Pins `HPS_IOB_1~3` and `HPS_IOB_5~7` (6 pins in total) are physically dedicated to the HPS SD Card/eMMC interface. When configuring the HPS Pin Mux, users **must** assign these specific pins to the SD/eMMC interface function.

- **Clock Requirement:** A free-running 25 MHz clock must be provided to one of the HPS I/O pins.
- **Compilation Check:** After pin assignment, a full Quartus compilation is required to verify that the HPS I/O pin assignments differ from any conflicts and compile successfully.
- **Series resistors:** To minimize signal reflections and maintain signal integrity, series resistors with values of 20–30 ohms shall be placed on the high-speed signal traces of the USB (60 MHz) and Ethernet RGMII (125 MHz) interfaces. Refer to the Comet A13 Carrier schematic for reference implementation.

3.6 Reset Signals

- **SYS_HPS_RST_N:** Users must connect a HPS reset signal to SYS_HPS_RST_N to reset HPS on SOM.

3.7 Boot Configuration Signals

- **IMAGE_FACTORY:** This signal acts as the boot image selector, enabling dual-boot functionality for the SOM. It determines whether the system boots from the factory default image or a user-defined image.
 - ◆ **Factory Boot (Default):** When IMAGE_FACTORY is driven High or left Floating, the system is configured to boot from the Factory image.
 - ◆ **User Boot:** When IMAGE_FACTORY is driven Low, the system is configured to boot from the User image.

Note: For applications that do not require dynamic dual-boot switching, this signal should be tied High or left floating to ensure the system defaults to the Factory boot configuration.

3.8 Trace-length Matching between SOM and Carrier Boards

If the user needs to perform trace-length matching between SOM and carrier board to maintain differential-pair integrity and high-speed signal quality, they can refer to the “Comet-A13-SOM-trace-delay.xlsx” spreadsheet which provides the trace lengths and delay times for all signals on the Comet A13 SOM that connect to the B2B connectors.

Mechanical and Heatsink Design

4.1 Introduction

This chapter details the mechanical specifications and thermal design of the Comet A13 SOM. It covers physical dimensions, assembly procedures, and the integrated heat spreader. Additionally, it provides 3D CAD resources and guidelines for implementing custom passive or active cooling solutions.

4.2 Heat Spreader

The Comet A13 SOM is shipped with an **aluminum heat spreader**, which transfers heat from the major heat sources on the SOM to its large surface area. Users may attach either a **passive** or **active** heatsink onto the heat spreader according to their application requirements.

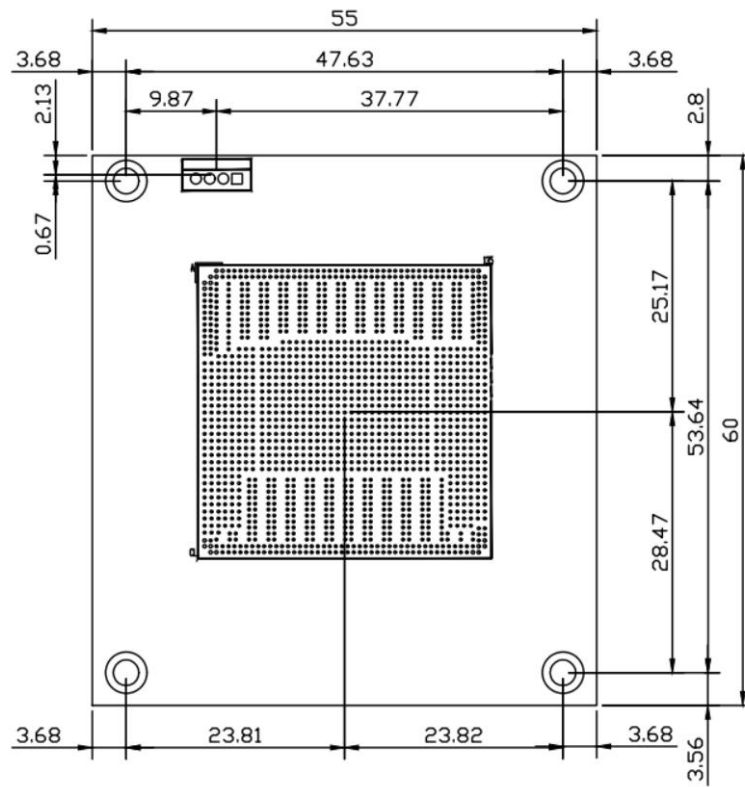
4.3 Mechanical Dimensions

The table below summarizes the mechanical specifications. Detailed dimensions are provided in the subsequent mechanical drawing.

Table 1-1 Comet A13 SOM Mechanical Specifications

Parameter	Specification
Length of SOM	60 mm
Width of SOM	55 mm
Height of SOM (with heatsink)	12.04 mm

- Mechanical Specifications of Comet A13 SOM without Heat Spreader (All dimensions in mm)



top view
All dimensions in mm

Figure 4-1 Top View

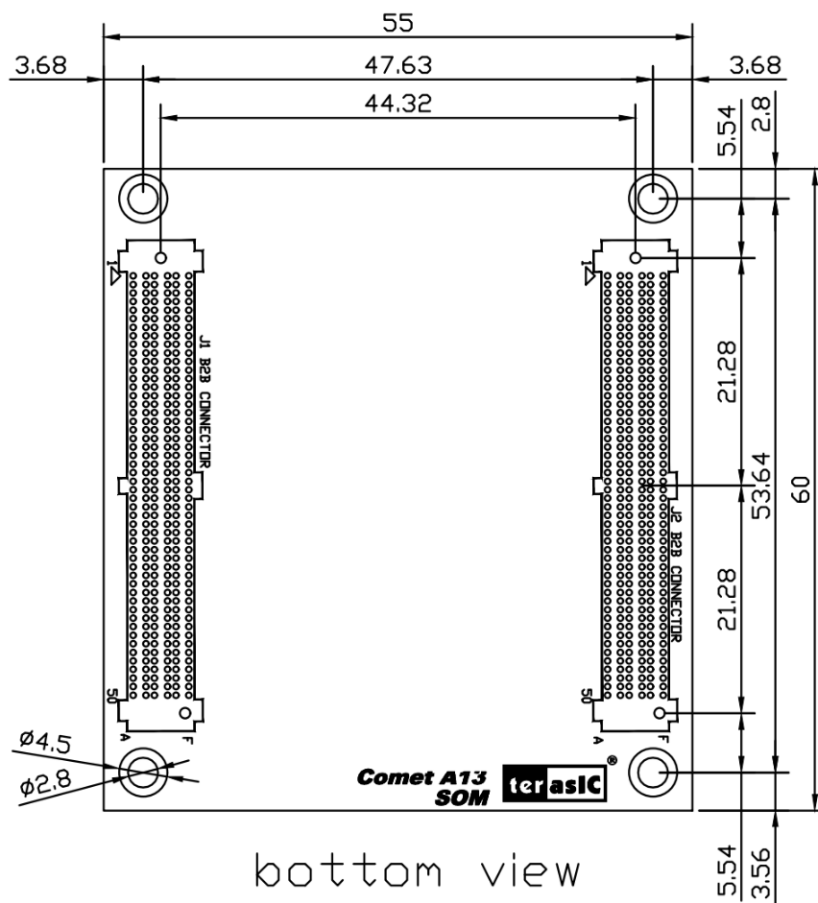


Figure 4-2 Bottom View

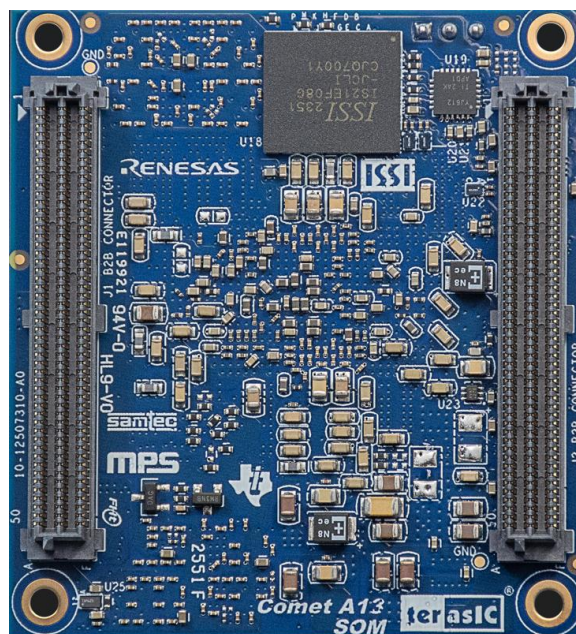


Figure 4-3 Comet A13 board bottom view

- The dimensions and details of the Comet A13 stand-offs

The following figures shows how the Comet A13 SOM and heat spreader may be attached to the carrier board using threaded stand-offs.

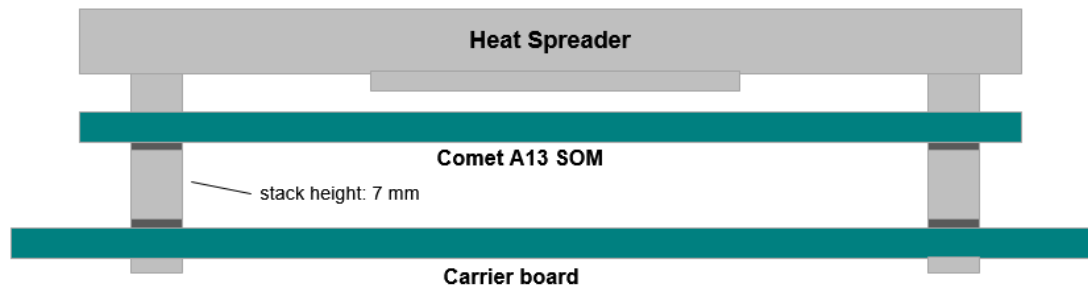


Figure 4-5 Mechanical Stack-up of Comet A13 SOM and Heatsink

The following figures shows the dimensions and details of Comet A13 threaded stand-offs.

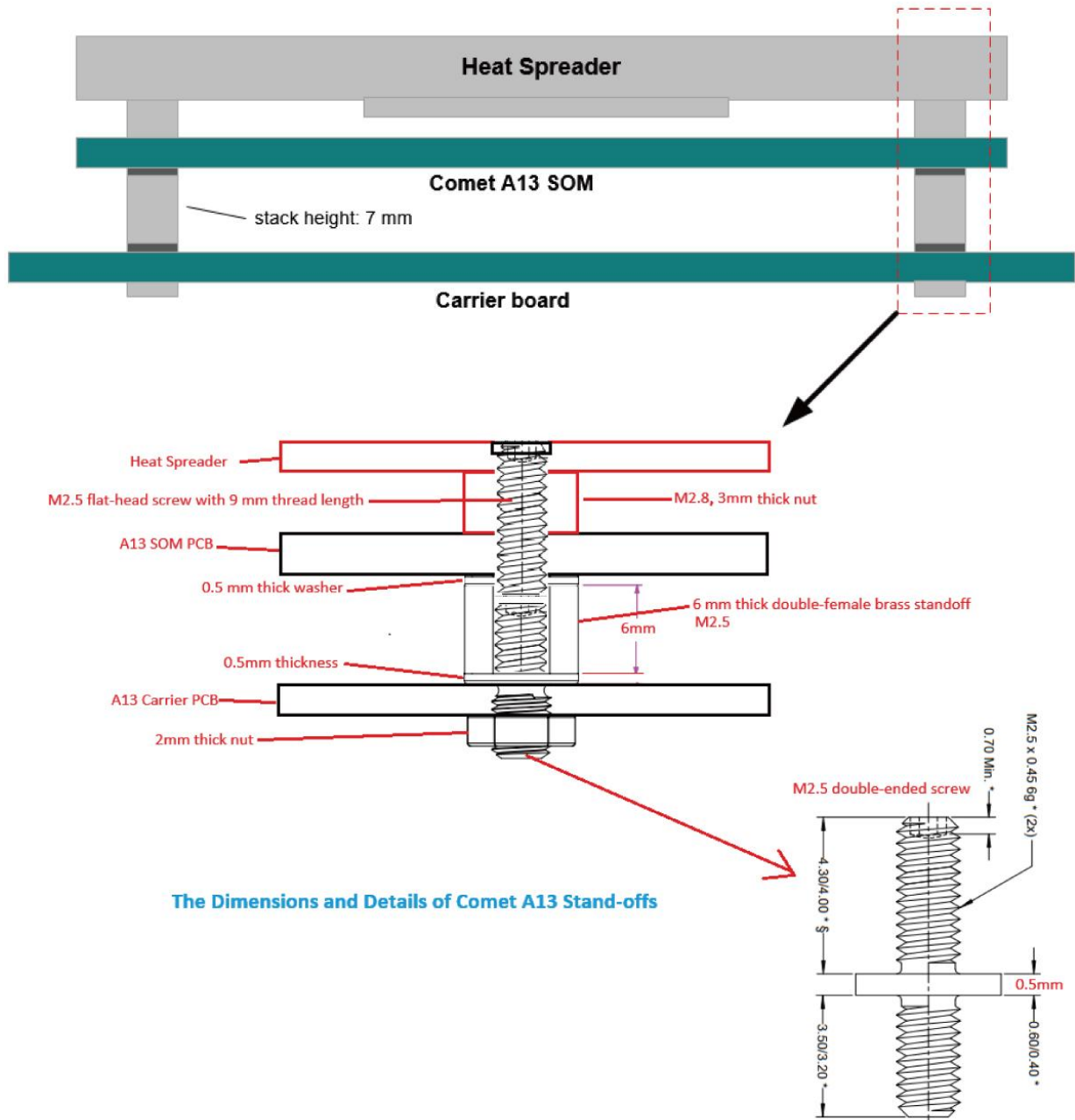


Figure 4-6 Detailed Assembly Diagram of Comet A13 SOM Stand-offs

4.4 Board-to-Board (B2B) Connector Orientation and Placement

To ensure proper mating between your custom carrier board and the Comet A13 SOM, designers must strictly follow the Board-to-Board (B2B) connector layout specifications. When placing the B2B connectors on your PCB layout, please refer to **Figure 4-7**.

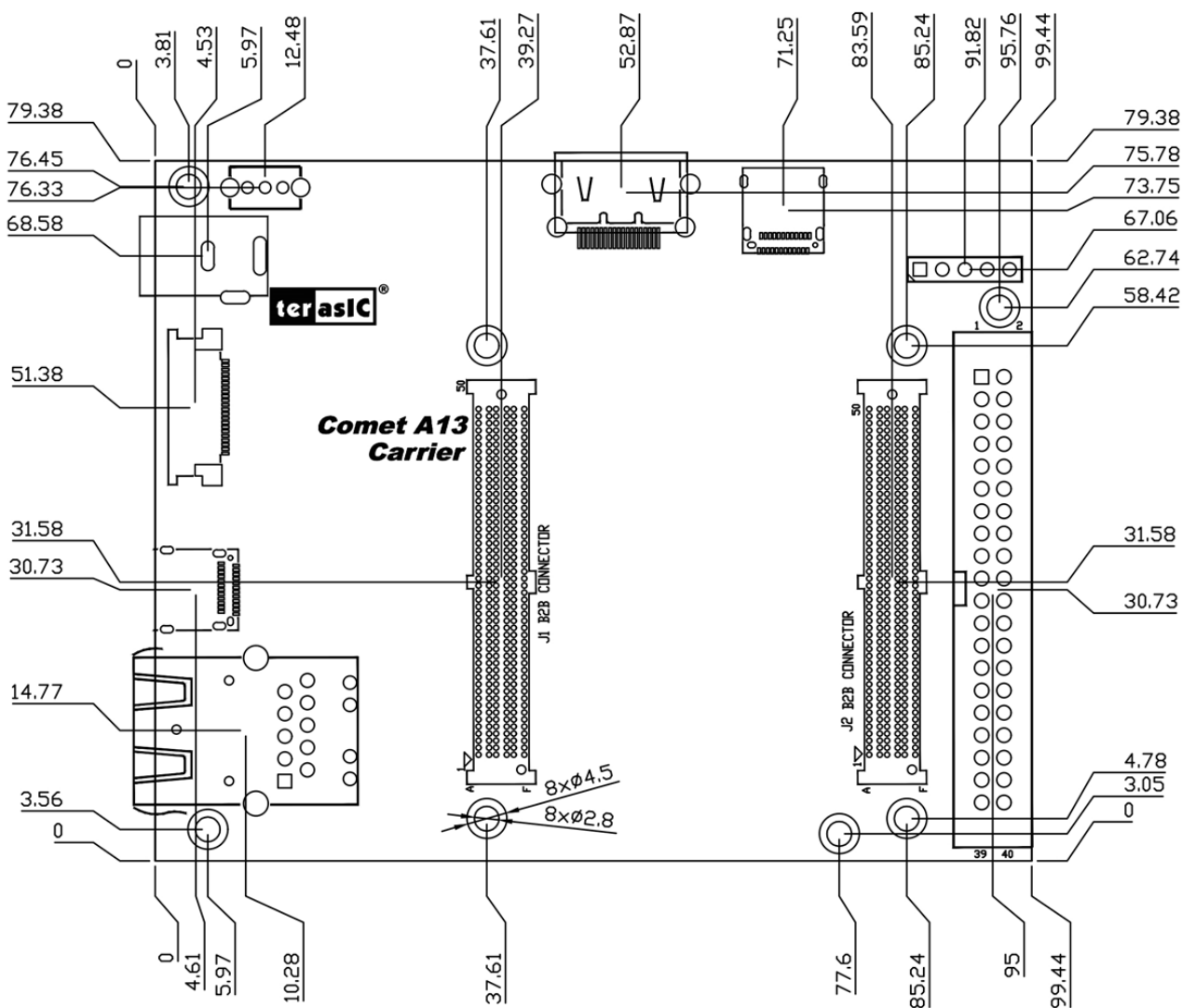


Figure 4-7 Terasic Carrier Board B2B Connector Layout

It is crucial to pay special attention to the following details to avoid reverse insertion or signal mismatch:

- **B2B Connector Numbering and Signal Definitions:** Ensure that the B2B connector numbering and signal definitions on your custom carrier board are consistent with the reference design. This is essential for proper connection with the Comet A13 SOM.
- **Pin 1 Location and Orientation:** Verify that the Pin 1 position aligns exactly as illustrated in the reference diagram.

⚠ WARNING: Failure to follow the specified connector numbering and Pin 1 orientation may result in mechanical mating failures or permanent damage to the SOM and the carrier board.

Chapter 5

Assembly & Disassembly

5.1 Assembly & Disassembly for SOM and Carrier

All the screws, washers, and standoffs required to assemble Comet A13 SOM and Carrier together will be pre-installed on the Comet A13 SOM. Here is an assembly and disassembly demonstration video of the SOM and Carrier for customer reference: <https://youtu.be/-NdPe7jFcs>

5.2 3D CAD Files

3D CAD models of the Comet A13 SOM are available for carrier board designers.

https://dl2.terasic.com/resources/cometa13/Comet_A13_revA_heatsink_3D_stp.zip

These files can be used to:

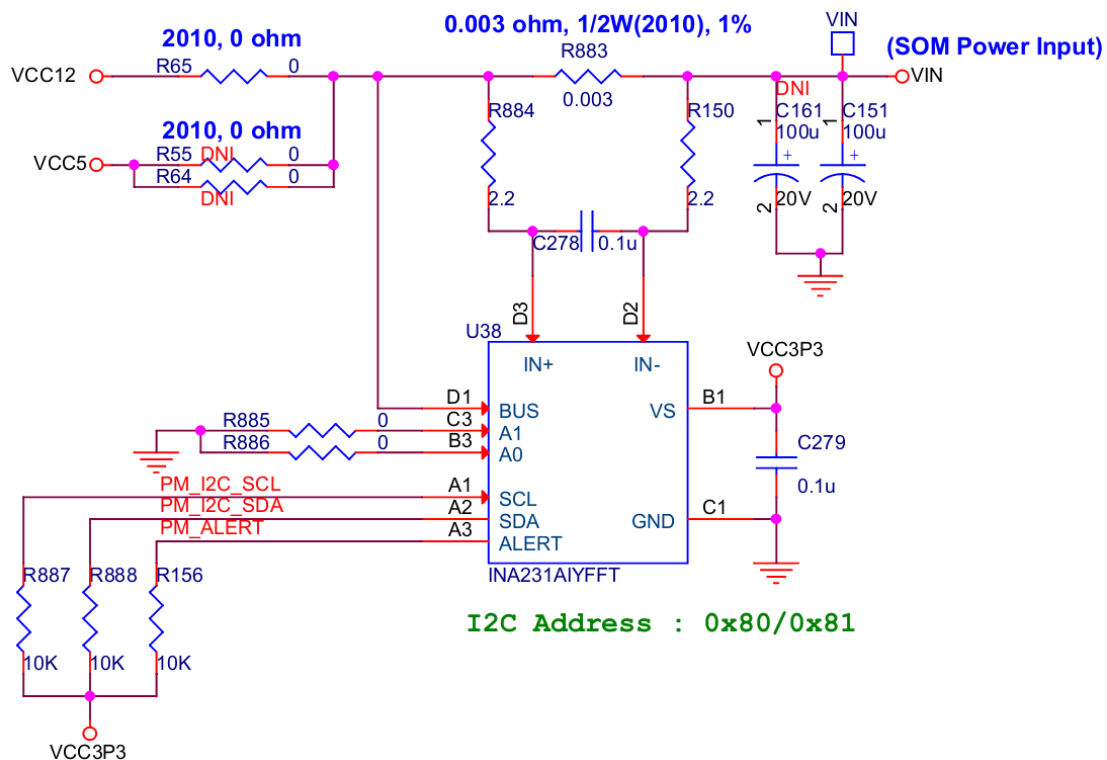
- Validate cooling solutions and heatsink designs.
- Check for system-level assembly interferences.
- Ensure proper alignment with B2B connectors.

Power Consumption Measurement

6.1 Power Monitoring System

Users can implement a power monitor circuit on the carrier board to measure SOM power consumption. By connecting the power monitor's I2C bus to the FPGA via the B2B connector, users can read power metrics.

- **I2C Address:** 0x80 / 0x81.
- **Schematic Reference:** Refer to the INA231 design example below:



Additional Information

Contact Terasic

Users can refer to the following table for technical support and more information of Terasic and our product:

Contact Method	Address
Email	support@terasic.com/sales@terasic.com
Tel	+886-3-575-0880
Website	www.terasic.com
Address	No.80, Fenggong Rd., Hukou Township, Hsinchu County, 303035 Taiwan

Revision History

Date	Version	Changes
2025.12	V1.0	First Version
2026.04	V1.1	Revise Figure 4-2 to include the pin 1 information of the B2B connector.
2026.04	V1.2	Add section 4.4 : Board-to-Board (B2B) Connector Orientation and Placement